MICROWAVE QPSK DEMODULATION TECHNIQUES
AT THE RECEIVER FRONT END

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Abstract

Quadriphase modulation of microwave or mm-wave carriers involves the rapid shifting of the phase of the carrier between one of four orthogonal positions by binary data included on two parallel data streams. The received quadriphase (QPSK) carrier can be demodulated by mixing this carrier with an appropriately phased local oscillator signal in a doubly-balanced mixer. One of the problems in demodulation of quadriphase carriers is the generation of the local oscillator having carrier frequency and phase information. This can be accomplished either at RF from the incoming QPSK carrier or at baseband by comparing the crosstalk associated with the two demodulated data streams. This paper will describe the applicable microwave technologies utilizing special quadrupler frequency multipliers which provide microwave carrier reconstruction which facilitates the demodulation of data information from the carrier.

Introduction

In a quadriphase system, two parallel data streams are used to develop four orthogonally separated phase states of phase information which correspond to the switching levels of the simultaneous component data streams and form a quadriphase or QPSK carrier. In order to demodulate the carrier at a receiver, a local oscillator following the phase of the incoming carrier must be developed using a carrier reconstruction loop. The heart of this loop is a special X4 frequency quadrupler which is the basis of this presentation.

QPSK Systems

A QPSK modulator for, say 500-Mbps systems will apply the two-component, 250-Mbps bit streams to phase-shift-keyed (PSK) modulators, respectively, and form the QPSK carrier by combining the two PSK carriers. This can be accomplished by use of either a parallel or a serial modulator to produce the four phases ($0°$, $90°$, $180°$, and $270°$) with less than a few degrees of ambiguity. The process of switching phase in two quadrature phase extremes of a QPSK carrier in a billionth of a second (1 nsec) which is 20% of a bit period of a 250 Mbps data stream, then imposes stringent requirements of phase shift accuracy (less than $2°$ in $180°$), phase balance (less than $3°$), and circuit group delay (group delay distortion of less than 0.2 nsec) across the modulator and output amplifier/frequency translator full bandwidth.

In the QPSK demodulation process, the QPSK carrier is sampled by the oscillator of the carrier reconstruction loop in each of a pair of doubly-balanced mixer-modulators whose LO carrier phases are in phase quadrature to regain each baseband data stream. Two principal types of carrier reconstruction loops are used for QPSK demodulation: 1) the frequency quadrupling loop, and 2) the Costas loop or I-Q loop. These two modulator systems are shown in Figs. 1a and 2. The I-Q loop generates a reference carrier locked in phase to either of the two possible received signal phases by providing both in-phase and phase-quadrature phase comparison at baseband to provide an error voltage which locks a phase-lock loop. The X4 carrier reconstruction loop uses frequency quadruplers to lock a phase-locked reference carrier oscillator. The data modulation is removed by the fourth-harmonic operation since any multiple of $90°$ when multiplied by four yields $0°$ (modulo $360°$).

At 0.5-Gbps data rates, a comparison of the X4 and IQ carrier reconstruction techniques, which normally favors the IQ system and which avoids the phase noise inherent in the use of the frequency quadrupler, is resolved from strictly circuit considerations. The X4 frequency multiplier is the principal circuit which must be optimized. However, for such wide bandwidths, the conversion efficiency is low and the SNR of the recovered reconstructed carrier may be
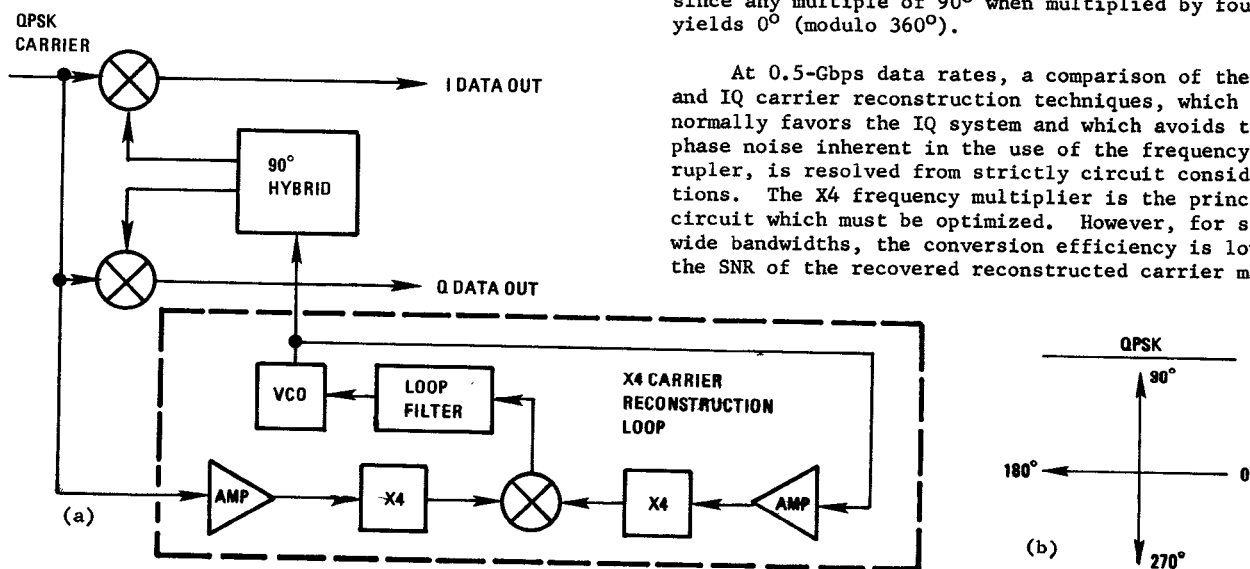

Fig. 1   (a) Frequency Quadrupling (X4) QPSK Demodulator; (b) Orthogonal Phase States of a QPSK Carrier

relatively low, requiring the coherent receiver phase-locked oscillator to be designed to avoid locking on a sideband of the recovered carrier.

The IQ carrier reconstruction, on the other hand, with its seemingly simpler circuit philosophy, depends on baseband signal processing and must rely upon wideband video amplifiers, low-pass filters, limiters, and quadrature detectors. This multiplicity of circuits will result in a large number of data addition or subtraction points that, by their multiplicity, introduce problems of noise, crosstalk, and circuit reflections which can significantly increase the basic signal-to-noise ratio of the receiver phase-lock loop system. The recovered baseband data streams at the output of each demodulation are passed through a matched filter and regenerated.
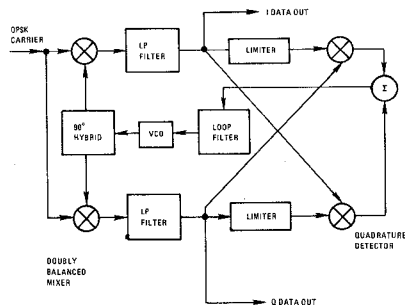

Fig. 2 Compound Costas Loop QPSK Demodulator

Types of QPSK X4 Multipliers

The frequency quadrupler or X4 multiplier operates in a mode wherein the four orthogonal vectors of the QPSK carrier shown in Fig. 1(b) are rotated by the X4 multiplier to all fall up on the reference or zero degree vector at the output of the multiplier. This then recreates a reference phase vector from the four vectors.

The X4 QPSK multiplier is in many ways different from the standard frequency quadrupler. Its input bandwidth must accommodate the full main-lobe of QPSK carrier spectrum, which is numerically equal in bandwidth to the QPSK data rate; i.e., a 500-megabit QPSK carrier including data from two component 250 megabit data streams will have a 500 MHz bandwidth.

The output circuit, on the other hand, must be very narrowband - of the order of a few megahertz to select the recovered carrier-phase vector from the modulation components which will occur at the multiplier output.

Efficiency of a QPSK X4 multiplier is not of primary importance. As shown in Fig. 3, amplifiers using transistors, FET's, or semiconductor diodes such as Gunn or Impatt diodes can be used to raise the output of the severely filtered output of the multiplier to a useful level to drive a mixer, of the order of zero dBm.
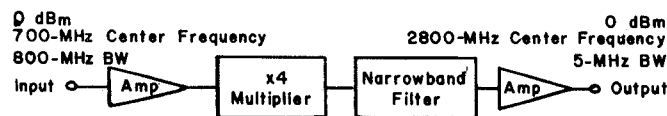

Fig. 3 Amplifier - X4 Multiplier - Filter/ Amplifier Complex

There presently exist several microwave techniques which are suitable for providing QPSK X4 carrier recovery, i.e.:

- X4 multipliers using step recovery diodes with wideband input circuits and ultra-narrowband output circuits.

- Tapped delay line frequency multipliers.

- Transistor or FET quadruplers using the non-linearity of the transistor or FET to deliver a fourth-harmonic output.

These techniques will be discussed in the following paragraphs. Most present day carrier recovery loops operate at IF frequencies from 70 MHz to 8 GHz, depending on the data rate and the system being used. Here, the X4 QPSK multiplier using step-recovery diodes are the most commonly used. However, the simplicity of the tapped delay line will make it useful in many systems, and the transistor multiplier, though complex, provides a means to simultaneously amplify the QPSK carrier and to develop a reference carrier which can be used to lock a phase-locked loop.

X4 QPSK Multiplier Using Step Recovery Diodes

The X4 multiplier using step recovery diodes is the most simple quadrupler to implement using standard multiplier circuit technology.

Fig. 4 shows a simple X4 multiplier which follows closely the basic circuit approaches used by G. Schaffner and J. Cochran. Here a wideband matching network is coupled to a shunt step recovery diode; a capacitance coupling is used to provide a series resonant coupling of the fourth harmonic developed across the diode to an output filter network.
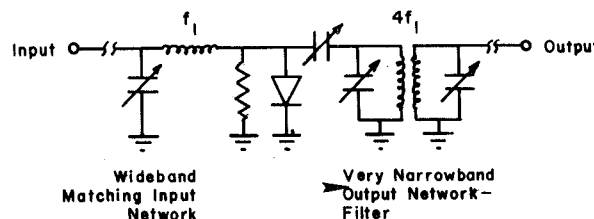

Fig. 4 X4 QPSK Multiplier Using a Step Recovery Diode

Such a circuit can be built using existing techniques from VHF to K-band and, since most carrier reconstruction loops operate in L-band and S-band, the multiplier can be built for achieving maximum amplitude of the recovered carrier from the QPSK carrier and not for efficiency. In fact, for a X4 QPSK multiplier operating from 700 MHz to 2800 MHz, efficiencies less than 5% were measured. For X4 multipliers operating in the unique mode from 1.7 GHz to 6.8 GHz efficiencies in excess of 10% were measured.

Figs. 5a and 5b show the output spectra of a X4 step recovery multiplier prior to final filtering. This multiplier accepts an input at 700 MHz and delivers an output at 2800 MHz. For a relatively low data rate of 50 Mbps, the recovered carrier was 30 dB greater than the largest of the surrounding modulation components. At 400 Mbps, the recovered carrier was 17 dB greater than the largest of the surrounding modulation components (noise). 17 dB is still a sufficiently large S/N ratio to lock the phase locked

Fig. 5a
Output of X4
multiplier due to
input of QPSK 700-
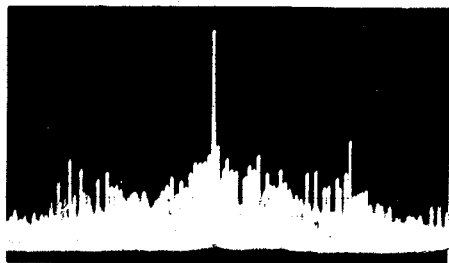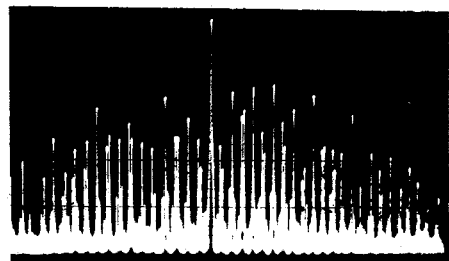MHz carrier at
50-Mbps rate.

Fig. 5b
Output of X4
multiplier due to
input of QPSK 700-
MHz carrier at
400-Mbps rate.

A tapped delay-line QPSK X4 multiplier was built for 700 MHz to 2800 MHz operation, using standard glass encapsulated mixer diodes. A conversion loss of around 30 dB was experienced but a reconstructed carrier with minimum modulation noise was achieved which was easily filtered and amplified to the zero dBm level. As long as 30 dB of gain is achievable in MIC amplifier chips at the output frequency, such a circuit is the simplest to build - up to frequencies well into K-band.

X4 QPSK Transistor Amplifier-Multipliers

One potentially important candidate for X4 QPSK carrier recovery is the transistor amplifier operated as both an amplifier and as a frequency quadrupler. Such a device was proposed in 1965 for microwave power generation by H. Lee and R. Minton, and was then ignored in favor of other microwave devices with far less complexity for power generation.

However, the transistor amplifier-multiplier using either bipolar transistors up to 6 GHz or FET's into the mm-waves at relatively low levels is an ideal candidate for MIC componentry and miniature circuitry by (1) utilizing the ability to match to a transistor over very wide bandwidths, (2) by using the nonlinear collector-to-base capacitance as the harmonic generating mechanism, and (3) by properly terminating the second harmonic at the collector - while coupling the collector to a narrowband resonator tuned to the carrier fourth harmonic.

References

1. C. L. Cuccia and W. Lee, "PSK Modulation and Demodulation", Paper 72-532, AIAA 4th Communications Satellite Conference, Washington, D.C., 1972.

2. G. Schaffner, "High Power Varactor Diodes", Motorola Application Note AN-147.

3. H. Lee and R. Minton, "Designing Transistor Multipliers", Microwaves, Nov. 1965.

oscillator. At data rates above 500 Mbps, the recovered carrier level was only 10 dB above the noise and operation of the phase locked loop would have been marginal and the probability of locking onto an incorrect side component would have been great.

It is clear that for very high data rates above 400 Mbps, the 700 MHz IF was inadequate to recover the carrier without false sideband lock, and a move to a much higher IF frequency would have been required.

Tapped Delay Line Multiplier

One interesting technique for developing a fourth harmonic reconstructed carrier from a QPSK carrier and by far the simplest technique, is the tapped delay line shown in Fig. 6. Here, a series of diodes are connected to a tapped delay line, made up of lengths of miniature cable. The input waveform has a period equal to the length of the delay line; the output waveform has peaks corresponding in number to the number of taps on the line. For a frequency quadrupler, four taps with four diodes were used.
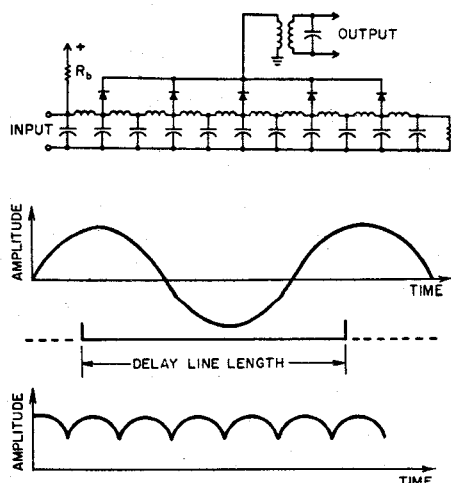

Fig. 6   Tapped Delay Line Frequency Multipliers
and Typical Input and Output Amplitude
Curves